AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

1. (Previously Presented) A computer readable medium having a program, the program performing a method for monitoring an execution of another program that is executable on at least one microprocessor of a micro controller using a debug logic of the micro controller, comprising:

causing the debug logic to trigger an exception upon access to a specific address range during a program execution time;

causing the at least one microprocessor to configure the debug logic; and

causing the debug logic to execute an exception routine after the exception is triggered during the program execution time;

wherein the access to the specific address range includes access to an illegal storage area, and

wherein the debug logic and its registers are operated in parallel to the program execution time to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack, so as to provide a secure stack check without using the program execution time of the microprocessor;

wherein the debug logic monitors a program run.

2. (Previously Presented) The computer readable medium according to claim 1, wherein:

the exception corresponds to an interrupt of the execution of the program.

3. (Previously Presented) The computer readable medium according to claim 1, wherein:

the debug logic is configured during a startup of the micro controller.

4. (Previously Presented) The computer readable medium according to claim 1, further comprising the step of:

during the execution of the exception routine, performing the steps of:

resetting the micro controller,

starting up the micro controller again, and

initializing the program.

5. (Previously Presented) The computer readable medium according to claim 4, further comprising the step of:

storing at least a type of a fault in a fault memory before the micro controller is reset and started up again and before the program is initialized.

6. (Previously Presented) The computer readable medium according to claim 5, further comprising the step of:

storing a memory address that was accessed before an occurrence of the fault in the fault memory before the micro controller is reset and started up again and before the program is initialized.

7. (Previously Presented) The computer readable medium according to claim 1, wherein:

the debug logic monitors whether the program accesses a preselectable address range of a memory during the program execution time.

8. (Previously Presented) The computer readable medium according to claim 7, wherein:

the debug logic monitors whether the program accesses an address range of a stack of the micro controller beyond a preselectable maximum stack size during the program execution time.

9. (Previously Presented) The computer readable medium according to claim 1, wherein:

the debug logic monitors whether an attempt is made during the program execution time to execute a code sequence of the program, swapped out from a flash memory of the micro controller into a random access memory of the micro controller, in the flash memory.

10. (Previously Presented) A control element for a micro controller, comprising:

an arrangement for storing a program, the program being executable on at least one microprocessor to perform the following:

causing a debug logic to trigger an exception upon access to a specific address range during a program execution time,

causing the at least one microprocessor to configure the debug logic, and

causing the debug logic to execute an exception routine after the exception is triggered during the program execution time;

wherein the access to the specific address range includes-access to an illegal storage area, and

wherein the debug logic and its registers are operated in parallel to the program execution time to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack, so as to provide a secure stack check without using the program execution time of the microprocessor;

wherein the debug logic monitors a program run.

11. (Original) The control element according to claim 10, wherein:

the control element corresponds to one of a read-only memory and a flash memory.

12. (Original) The control element according to claim 10, wherein:

the micro controller is arranged in a motor vehicle.

13. (Previously Presented) A micro controller, comprising:

at least one microprocessor;

a debug logic, wherein:

a program is executable on the at least one microprocessor,

the debug logic monitors an execution of the program during a program execution time and triggers an exception upon access to a specific address range, and

the at least one microprocessor configures the debug logic; and

an arrangement for executing an exception routine after the exception is triggered during the program execution time;

wherein the access to the specific address range includes-access to an illegal storage area, and

wherein the debug logic and its registers are operated in parallel to the program execution time to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack, so as to provide a secure stack check without using the program execution time of the microprocessor;

wherein the debug logic monitors a program run.

14. (Original) The micro controller according to claim 13, wherein:

the exception corresponds to an interrupt of the execution of the program.

15. (New) The micro controller according to claim 13, wherein:

a memory address is stored that was accessed before an occurrence of the fault in the fault memory and at least a type of a fault is stored in a fault memory, before the micro controller is reset and started up again and before the program is initialized,

during the execution of the exception routine, the micro controller is reset, the micro controller is started up again, and the program is initialized,

the exception corresponds to an interrupt of the execution of the program,

the debug logic is configured during a startup of the micro controller,

the debug logic monitors whether the program one of (i) accesses a preselectable address range of a memory during the program execution time, and (ii) accesses an address range of a stack of the micro controller beyond a preselectable maximum stack size during the program execution time, and

the debug logic monitors whether an attempt is made during the program execution time to execute a code sequence of the program in a first type of memory, swapped out from the first type of memory of the micro controller into another type of memory of the microcontroller.

16. (New) The computer readable medium according to claim 1, wherein:

a memory address is stored that was accessed before an occurrence of the fault in the fault memory and at least a type of a fault is stored in a fault memory, before the micro controller is reset and started up again and before the program is initialized,

during the execution of the exception routine, the micro controller is reset, the micro controller is started up again, and the program is initialized,

the exception corresponds to an interrupt of the execution of the program,

the debug logic is configured during a startup of the micro controller,

the debug logic monitors whether the program one of (i) accesses a preselectable address range of a memory during the program execution time, and (ii) accesses an address range of a stack of the micro controller beyond a preselectable maximum stack size during the program execution time, and

the debug logic monitors whether an attempt is made during the program execution time to execute a code sequence of the program in a first type of memory, swapped out from the first type of memory of the micro controller into another type of memory of the microcontroller.

17. (New) The control element for the micro controller according to claim 10, wherein:

a memory address is stored that was accessed before an occurrence of the fault in the fault memory and at least a type of a fault is stored in a fault memory, before the micro controller is reset and started up again and before the program is initialized,

during the execution of the exception routine, the micro controller is reset, the micro controller is started up again, and the program is initialized,

the exception corresponds to an interrupt of the execution of the program,

the debug logic is configured during a startup of the micro controller,

the debug logic monitors whether the program one of (i) accesses a preselectable address range of a memory during the program execution time, and (ii) accesses an address range of a stack of the micro controller beyond a preselectable maximum stack size during the program execution time, and

the debug logic monitors whether an attempt is made during the program execution time to execute a code sequence of the program in a first type of memory, swapped out from the first type of memory of the micro controller into another type of memory of the microcontroller.